SEGA™

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Consumer Products Division

32X
Hardware Manual
Supplement 1

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32X Hardware Manual Supplement 1

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1. About the 32X System Register

The 32X system register can cause a mistake in reading if simultaneously performing read and write from the 68000 and SH2. However, except for the communication and PWM registers, since there are many registers that can not access from both 68000 and SH2, or from 68000 to SH2, even when reading and writing at the same time, the read side will continue reading two times, and it will be determined that correct data is being read when they coincide.

Development boards until the Target ver. 1.1, and the ver. 2.0 development board initially shipped, could simultaneously read and write from both directions; but not the versions of development boards and devices since then. This is because the design that originally allowed read and write bidirectionally had to be functionally cut due to the chip size. As a result, be aware that the development board and device may not operate even by the program currently operating.

On the following page is an example of a communication register in which read and write are frequently done at the same time. A problem to be aware or with simultaneous read/write are system registers that can similarly read and write from other opposite directions, and not necessarily the communication register. The 32X has 8-word communication registers which are able to write in byte and word units; however, when accessing the same address please note the following points.

1) The same address can be read simultaneously from both SH2 and 68000.
2) When writing the same address simultaneously from both SH2 and 68000, one of the values is written, but which one can not be predicted since it is controlled by write timing. However, there is no problem in accessing the same address simultaneously when divided by byte units, one direction significant 8-bit and the other direction insignificant 8-bit.
3) When simultaneously reading, on the one hand, and writing, on the other hand, the same bytes or words of the same address from both the SH2 and the 68000, the write process will definitely occur but mistakes may occur in the read process. This is due to the fact that the time in which data written on one side is transferred to the other side within the I/F chip differs according to the bit. But there is no problem in accessing the same address simultaneously when divided by byte units, one direction significant 8-bit and the other direction insignificant 8-bit.

Example

Assume that 68000 uses communication register A15120H and transports instructions to SH2. SH2 always reads 4020H and performs various operations from values written by commands. There are three types of written values: FFFFH, AAAAH, and 5555H. SH2 receives commands, clears by writing 0000H when the operation ends, lets the 68000 know when the operation ends, and waits for the next command. If at that time 68000 writes FFFFH and SH2 is simultaneously reading, SH2 can read which ever value of 0000H ~ FFFFH. AAAAH or 5555H commands can then be executed. To avoid this, the address that reads and writes directly in both sides in the communication register requires data of only 1 bit inside 1 word. In other words, one bit can only have one meaning. If with respect to the data that is already written and the data that is to be written next, the set up does not allow a single to change, then errors could occur. In this example,

a) Miss-reading can be avoided by using a data format that has 1 bit in 1 word such as instruction commands 8000H, 4000H, and 2000H. But in this case only 16 types of commands can be transferred.
b) Command writes to A15122H, and A15120H gives a flag that shows simple command write. After a command is written to A15122H, 68000 writes 0001H to A15120H. SH2 writes 0000H to 4020H when the operation ends.

2. About FIFO

The configuration of FIFO is 4 words X 2 of block A FIFO and block B FIFO. Figure 1 shows the actual configuration. (The original configuration differs considerably but this configuration should be thought of as a type.) The operation is explained next. When FIFO is used, fetch DREQ by active H and edge, set the dual address mode and transfer destination to 4012H, then put the 1 time transfer size in word units. DACK is not used with the I/F chip, therefore any setting is all right. FIFO should be used in 4-word units. The 68000, after each kind of register of the DREQ relationship has been set, sets the DREQ control register in response to the transfer type.

The 68000 directly writes to FIFO and A1512H the data that you want to be transferred to SH2 . FIFO block A is written to first because it is the first selected. Because all of FIFO block A is filled at the time 4 words are written, the write destination is switched to FIFO block B. After which, a FIFO block is switched each time it is filled. Further, for each 4 words written, the 68000 should write the next 4 words after confirming whether A15106H, bit 7 of the DREQ control register, and FIFO Full are 0. An operation in which more is written while FIFO is full becomes undefined. The I/F chip sets DREQ 0 in SH2 to H and activates DMA at the step that 1 FIFO block and 4 words are full. SH2 reads 4012H and FIFO by DMA, and the DREQ 0 output of the I/F chip becomes L. After this, DREQ 0 becomes H until the FIFO block, following a minimum 3 times in one direction, is empty. When 4 DMA transfers end, the SH2 read FIFO block switches. DREQ 0 becomes H when all the switched FIFO blocks are written by the 68000, and the DMA transfer request is

sent again as previously mentioned. The operation on the previous page is then repeated until DMA transfer is done the number of times that the length is written to A15110H and 68 to SH DREQ Length. FIFO Full occurs when 68000 selects the block that SH2 is reading or is going to read to the write destination. When all transfer of the 68000 side has ended, 68S of bit 2 of A15106H automatically becomes 0 and FIFO access of the 68000 side ends. Then 68000 ignores anything written to A15112H and FIFO. DMA transfer requests are sent by DREQ 0 until all DMA transfer for SH2 have ended. Thus, the communication register should be used when SH2 side request end must be reported from the SH2 side to 68000 since it is not known whether or not DMA transfer of the SH2 side has ended, even if 68S is 0. If 68S becomes 0 while 68000 is transferring, DMA transfer can be forcefully interrupted, but because the SH2 side DMA transfer, during that time, forces DREQ 0 to become L, operation after that is undefined. The value of the counter that indicates the write destination of FIFO itself is also undefined. Thus, only when systems such as VRESET are reset or when a SH2 side operation is controlled by 68000 should you use DMA forced end by writing 0 to 68S. On the other hand, when a system has been reset, 68S force-clear of the transfer in progress can be performed and you should, therefore, write a 0 to 68S.

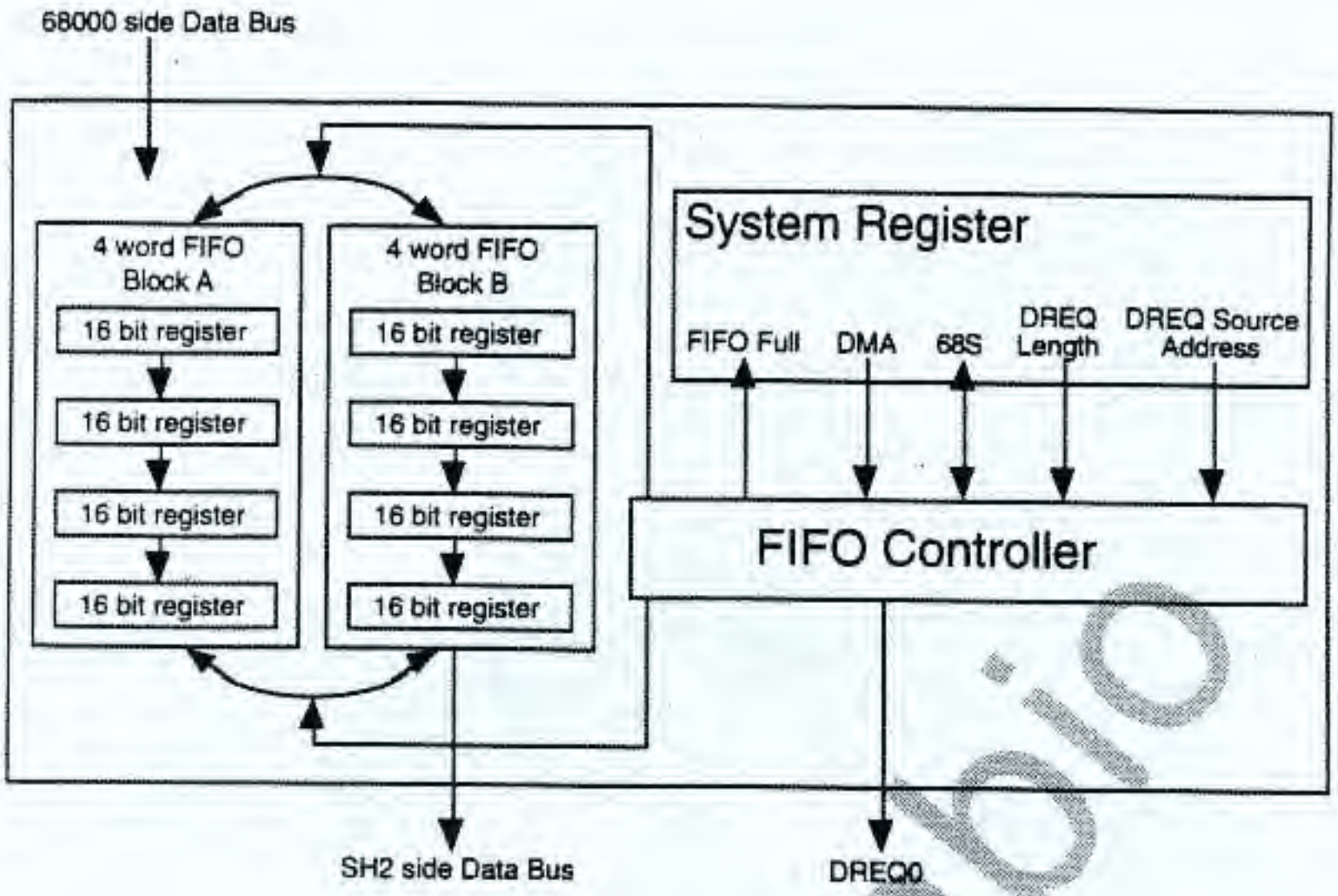

Fig. 1 Configuration of 4 Word X 2 FIFO

3. About VDP Access

The 32X VDP is done through the VDP I/F circuit of the I/F chip to the VDP chip. VDP switches access of the 68000 and SH2 simply by A15100H (4000H for SH2) of bit 15 and the FM bit. Figure 2 shows a block diagram of the SH2, 68000, I/F chip and VDP chip. The SH2 side has a 2 word write cache for the frame buffer and can actually write up to a continuous 4 words by 3 clocks existing in the minimum cycle during the external access of SH2. Reading to other VDP registers, palettes, and all VDP requires at least 7 clocks. When reading to the VDP or writing to the VDP register and palette immediately after writing to the frame buffer, after all the data currently in the cache is transferred to the VDP side, compared to a normal independent access, a large number of waits are entered against the SH2, thus prolonging the access time.

One point of caution is when, in the worst case scenario, transfer to the VDP becomes distorted and SH2, 68000, as well as the VDP, lock up because access authorization is forced to the 68000 side while the VDP I/F circuit is writing to the frame buffer for VDP if the FM bit is set to 0 immediately after SH2 finishes writing to the frame buffer. Accordingly, when switching the FM bit. it must be done after reading to the frame buffer, VDP register or palette (or writing to the VDP register and palette) and all cache data is transferred to the VDP.

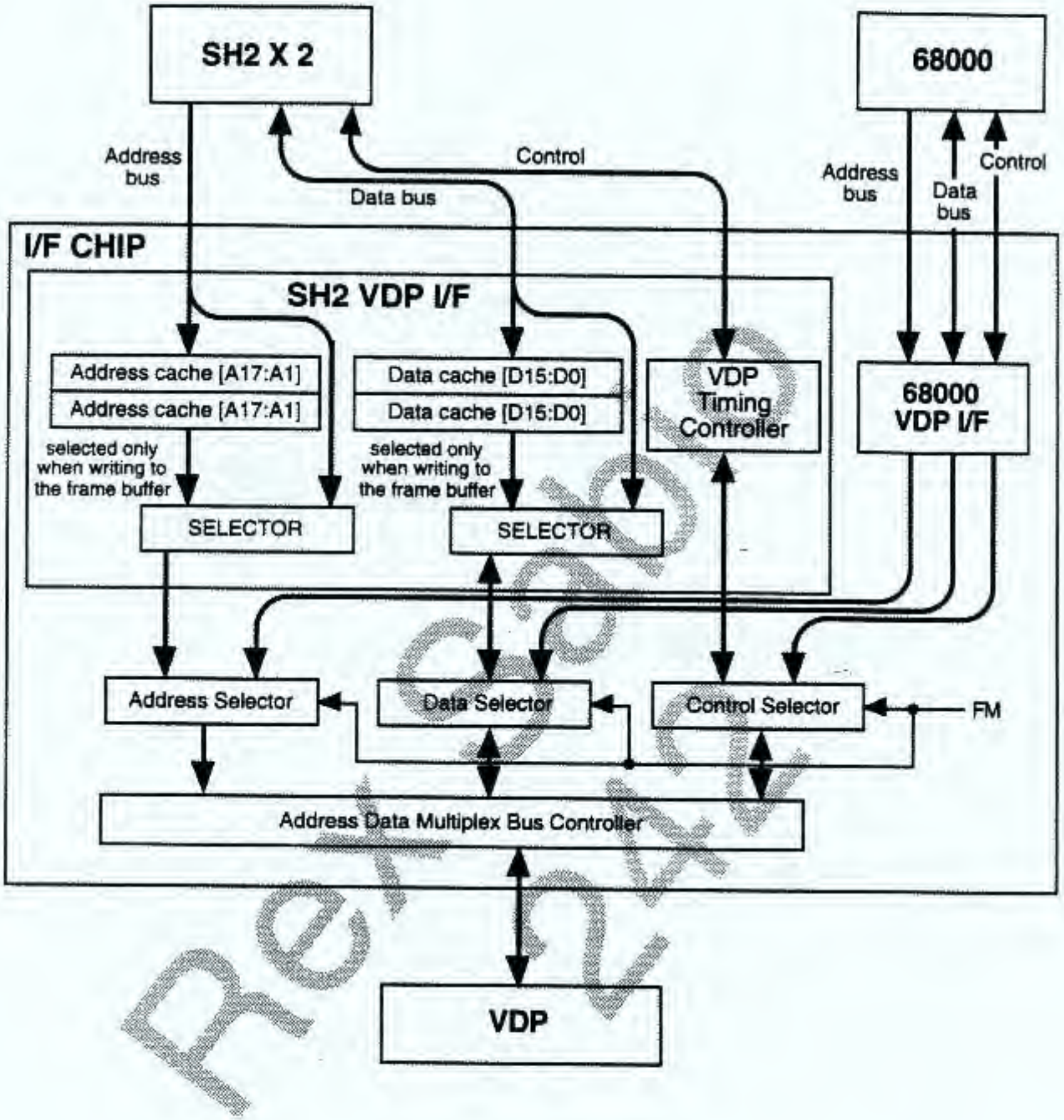

Fig. 2 Block Diagram of SH2, 68000, I/F Chip and VDP Chip